Modeling Via Hole Grounds in Microstrip

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Abstract—**A simple model for a cylindrical via hole in microstrip is presented. The model is based on a modification of the inductance of a cylindrical conductor as derived from Maxwell's equations. The model has been verified experimentally, and corroborated by other solutions using numerical techniques.**

I. Introduction

In a previous paper [1], one of the authors suggested that the inductance of a cylindrical via hole in microstrip similar to that shown in Fig. 1 was related to its diameter and length by

$$L_{\text{image}} = \frac{\mu_0}{4\pi}\left[2h \cdot \ln\left(\frac{2h + \sqrt{r^2 + (2h)^2}}{r}\right) + \left(r - \sqrt{r^2 + (2h)^2}\right)\right]. \quad (1)$$

This conclusion was based upon the assumption that the presence of a vertical components of current proximate to a ground plane required the inclusion of the image inductance. This relationship was obtained by using the inductance of a cylindrical conductor from [2], [3], replacing the length with twice the height of the via post, and halving the resulting inductance.

II. Comparison of Measurement to Theoretical and Numerical Results

Measurements indicated that the inductance values predicted by (1) were considerably higher than observed. As a first step, it was hypothesized that a cylindrical section without an image term would be a better approximation of the inductance. This relationship is given by

$$L_{\text{imageless}} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h + \sqrt{r^2 + h^2}}{r}\right) + \left(r - \sqrt{r^2 + h^2}\right)\right]. \quad (2)$$

The imageless inductance relationship resulted in noticeably lower values of inductance for the same via post. However, it was determined that the values predicted by both the image and imageless equations were significantly higher than those observed experimentally.

The imageless relationship was modified to better fit experimental data after performing an extensive set of numerical solutions of the via structure in Fig. 2, with a wide range of diameter to height (d/h) ratios. The analysis technique used was an integral formulation of the method of moments as implemented in the software program discussed in [4], [5].

The simulations were performed on microstrip vias in 100–635 μm substrates for $0.2 < d/h < 1.5$, $2.2 < \epsilon_r < 20$, and $1 < w/h < 2.2$. This range covers most practical dimensions of via holes in common microwave materials. The dimensions are limited on one extreme by the ability to metallize the via holes and on the other extreme by the via hole's undesirably large size.

The results of the numerical simulation agreed very closely with the measured data obtained for direct and resonator measurements of the structure shown in Fig. 1. It is also in excellent agreement with values obtained from other foundries [6] and other published results [7]. Simulations of similar topologies by other investigators using finite element techniques and other numerical methods were also in close agreement to our measured results [8], [9].

The results of the measurements and the numerical simulation indicate that the inductance of a cylindrical via hole can be represented as

$$L_{\text{via}} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h + \sqrt{r^2 + h^2}}{r}\right) + \frac{3}{2}\left(r - \sqrt{r^2 + h^2}\right)\right]. \quad (3)$$

Equation (3) represents an empirical factor change of the second term from 1 to 3/2. While there is a theoretical justification for this term, it has not yet been reconciled with the published derivation [2], [3] so that at this time it is sufficient to conclude that (3) is in close agreement with the numerical simulation and experimental data.

Fig. 3 relates the via inductance to the d/h ratio for substrate heights of 100, 200, 381, and 635 μm. A second graph is provided which has normalized the inductance to the substrate height and plots the inductance per unit length for all four substrate heights demonstrating the validity of the model for any d/h ratio.

The numerical simulations of the via structure suggested a small sensitivity of the inductance of the post to the dimensions of the via pad. However, this dependency was small, resulting in less than a 4% variation in the post inductance over a very large range of pad w/h dimensions, and has not been considered in the model.

The resistance of the via hole is highly dependent on

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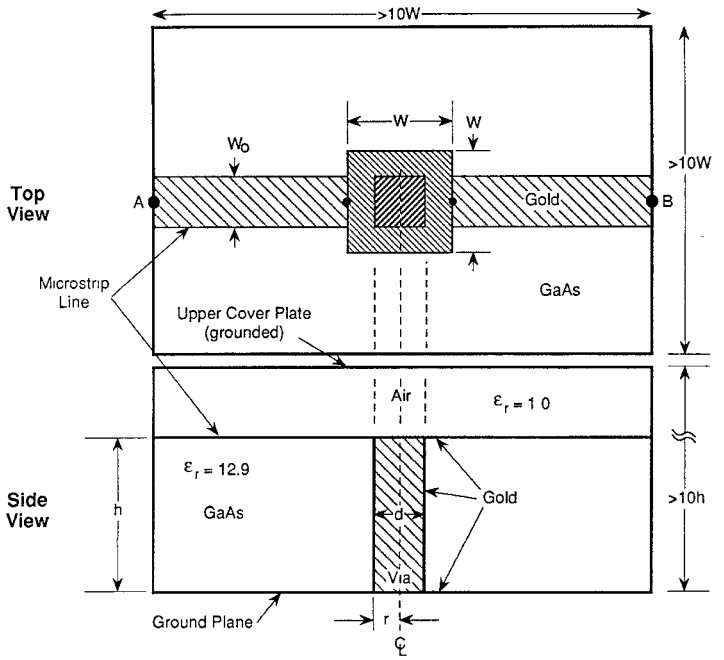

Fig. 1. Top and side views of a cylindrical via in microstrip.

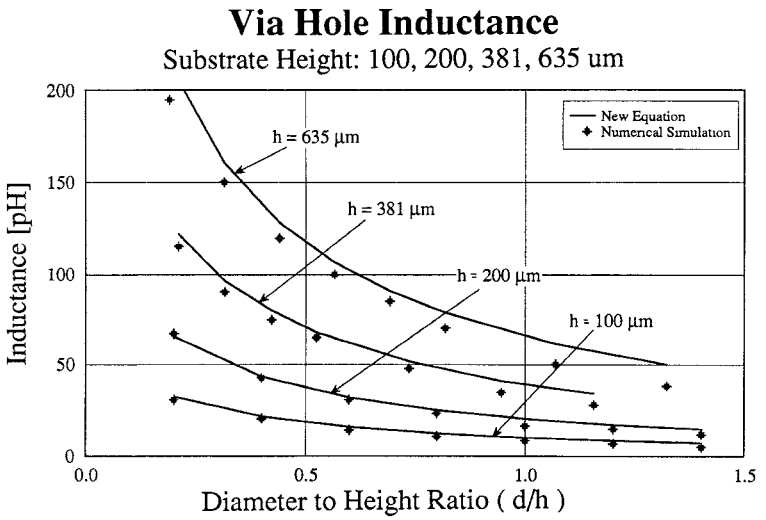

Fig. 2. Via hole inductance for substrate heights of 100, 200, 381, 635 μm.

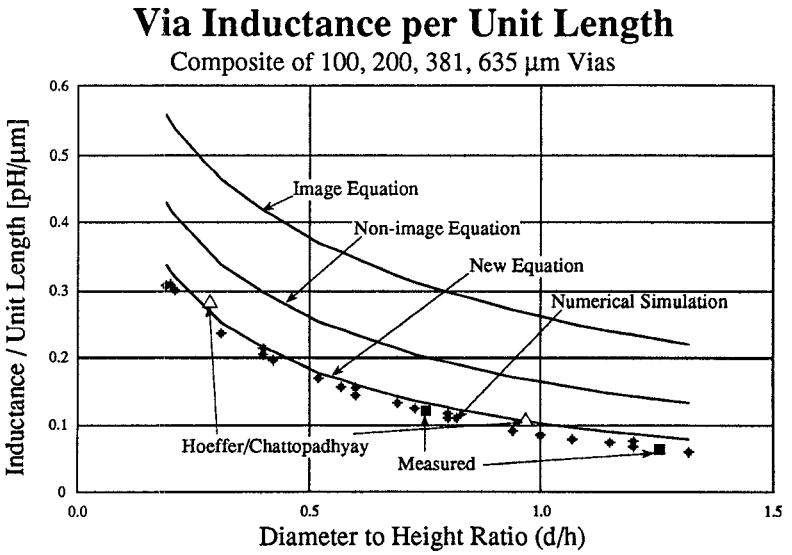

Fig. 3. Via hole inductance per unit length as a function of several equations and numerical simulation.

fabrication processes and may have to be considered at low frequencies [10]. The following relationship may be used as a close approximation to the via resistance and is valid independent of the ratio of the metalization thickness to the skin depth:

$$R_{\text{via}} = R_{\text{dc}} \sqrt{1 + \frac{f}{f_\delta}}, \tag{4}$$

where

$$f_\delta = \frac{1}{\pi \mu_0 \sigma t^2}.$$

III. Conclusion

A model has been presented for a cylindrical via hole in microstrip which has been verified numerically and experimentally. This model is useable for a range of $h < 0.03\lambda_0$ and is easily implemented in circuit CAE tools.

Via holes fabricated using conventional foundry techniques are actually conical rather than cylindrical sections. If the upper and lower diameters are not too different, however, the difference between the inductance values has been calculated to be small.

The inductance of the top pad is a *very* significant part of the total inductance of the via structure. The practical considerations of lowering the via post inductance by increasing the diameter of the hole usually are offset, at least in MMIC fabrication, by the necessity of a larger pad. The larger pad is to ensure reliable alignment during backside processing.

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